REMARKS

By the present amendment and response, claims 1, 7, 17, and 23 have been amended to overcome the Examiner's objections and claims 6 and 22 have been canceled. Thus, claims 1-5, 7-21, and 23-32 remain pending in the present application. Reconsideration and allowance of pending claims 1-5, 7-21, and 23-32 in view of the following remarks are requested.

The Examiner has rejected claims 1, 3-4, and 11-16 under 35 USC §103(a) as being unpatentable over U.S. patent number 6,261,467 to Giri et al. ("Giri") in view of U.S. patent number 6,077,765 to Kinichi Naya ("Naya") and U.S. patent number 6,100,589 to Kazuo Tanaka ("Tanaka"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 17, is patentably distinguishable over Giri, Naya, and Tanaka, singly or in any combination thereof.

The present invention, as defined by amended independent claim 1, teaches, among other things, a first conductor comprising interconnect metal and situated in a semiconductor die, a first isolation layer situated over the first conductor, a second conductor comprising under bump metal, comprising at least two conductor segments, and situated over the first isolation layer, and a second isolation layer situated over the second conductor, where the first conductor electrically connects the at least two conductor segments. As disclosed in the present application, a first conductor can be patterned in the last interconnect metal layer of a semiconductor die and covered by a first

isolation layer. As disclosed in the present application, a second conductor can be patterned from a first layer of under bump metal deposited over the first isolation layer. As further disclosed in the present application, vias can be formed in the first isolation layer to electrically connect the first and second conductors, which can form a passive component.

For example, the first and second conductors can form an inductor comprising windings on both the last interconnect metal layer of the semiconductor die and the layer of under bump metal. As a result, the present invention advantageously achieves an inductor having a lower parasitic capacitance and smaller size compared to typical off-die inductors. Additionally, by utilizing a layer of under bump metal to form an inductor, the present invention advantageously achieves an inductor having a lower resistance and superior quality factor compared to conventional on-die inductors. Moreover, by forming an inductor in a layer of under bump metal, the inductor achieved by the present invention can advantageously cover as much of the area on the top surface of the semiconductor die as required in a specific application

In contrast to the present invention as defined by amended independent claim 1, Giri does not teach, disclose, or suggest a first conductor comprising interconnect metal and situated in a semiconductor die, a first isolation layer situated over the first conductor, a second conductor comprising under bump metal, comprising at least two conductor segments, and situated over the first isolation layer, and a second isolation layer situated over the second conductor, where the first conductor electrically connects the at least two

conductor segments. Giri is directed to a ceramic carrier that can house IC chips or other surface mount components. Giri specifically discloses carrier 100, which includes conductor pattern layer 102, dielectric layer 108 situated over conductor pattern layer 102, wiring layer 110 situated on dielectric layer 108, and passivation layer 112 situated on wiring layer 110. See, for example, column 2, lines 31-46 and Figures 1 and 1A of Giri. In Giri, joining pads 118 are formed on wiring layer 110 and may provide suitable sites for mounting IC chips or other surface mountable components such as capacitors or resistors. See, for example, column 2, lines 54-62 and Figures 1 and 1A of Giri.

Thus, in Giri, conductor pattern layer 102, e.g. a first conductor, is situated in carrier 100 and not in a semiconductor die, as specified in amended independent claim 1. Furthermore, Giri fails to teach, disclose, or suggest a first conductor situated in a semiconductor die and comprising interconnect metal, a first isolation layer situated over the first conductor, and a second conductor situated over the first isolation layer, where the second conductor comprises at least two conductor segments and also comprises under bump metal, and where the first conductor electrically connects the at least two conductor segments. Moreover, Giri fails to teach, disclose, or suggest a second isolation layer situated over a second conductor comprising under bump metal. In fact, Giri does not even mention forming a conductor in a semiconductor die.

In contrast to the present invention as defined by amended independent claim 1, Naya does not teach, disclose, or suggest a first conductor comprising interconnect metal and situated in a semiconductor die, a first isolation layer situated over the first conductor,

a second conductor comprising under bump metal, comprising at least two conductor segments, and situated over the first isolation layer, and a second isolation layer situated over the second conductor, where the first conductor electrically connects the at least two conductor segments. Naya specifically discloses forming under-bump metallurgy ("UBM") layer 25 on bonding pad 22 and passivation layer 23, which are situated on substrate 21, and forming resist layer 26 over UBM layer 25. See, for example, column 4, lines 39-51 and Figure 2 of Naya. However, Naya fails to teach, disclose, or suggest a first conductor situated in a semiconductor die and comprising interconnect metal, a first isolation layer situated over the first conductor, and a second conductor situated over the first isolation layer, where the second conductor comprises at least two conductor segments and also comprises under bump metal, and where the first conductor electrically connects the at least two conductor segments. Thus, Naya fails to cure the basic deficiencies of Giri discussed above.

In contrast to the present invention as defined by amended independent claim 1, Tanaka does not teach, disclose, or suggest a first conductor comprising interconnect metal and situated in a semiconductor die, a first isolation layer situated over the first conductor, a second conductor comprising under bump metal, comprising at least two conductor segments, and situated over the first isolation layer, and a second isolation layer situated over the second conductor, where the first conductor electrically connects the at least two conductor segments. Tanaka specifically discloses a bonding pad including first electrode layer 300, first insulating interlayer 160 situated over first

electrode layer 300, and second electrode layer 200 situated over first insulating interlayer 160. See, for example, column 6, lines 20-24 and Figure 2B of Tanaka. In Tanaka, first electrode layer 300 is electrically connected to second electrode layer 200 by conductive layers 112b to 117b, which are embedded into through holes in first insulating interlayer 160. See, for example, column 7, lines 23-25 and Figure 2B of Tanaka.

However, Tanaka fails to teach, disclose, or suggest a first conductor situated in a semiconductor die and comprising interconnect metal, a first isolation layer situated over the first conductor, and a second conductor situated over the first isolation layer, where the second conductor comprises at least two conductor segments and also comprises under bump metal, and where the first conductor electrically connects the at least two conductor segments. Thus, Tanaka combined with Naya fails to cure the basic deficiencies of Giri discussed above.

For all the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is not suggested, disclosed, or taught by Giri, Naya, and Tanaka, singly or in any combination thereof. Thus amended independent claim 1 is patentably distinguishable over Giri, Naya, and Tanaka and, as such, claims 2-4 and 7-15 depending from amended independent claim 1 are, *a fortiori*, also patentably distinguishable over Giri, Naya, and Tanaka for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The present invention, as defined by amended independent claim 17, teaches a method for fabricating the structure disclosed in amended independent claim 1. Thus, for

reasons similar to those discussed above, amended independent claim 17 is also patentably distinguishable over Giri, Naya, and Tanaka. Thus, claims 18-20 and 23-21 depending from amended independent claim 17 are, *a fortiori*, also patentably distinguishable over Giri, Naya, and Tanaka for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The Examiner has further rejected claims 5 and 21 under 35 USC §103(a) as being unpatentable over Giri in view of Naya and Tanaka, and further in view of U.S. patent number 6,091,310 to Utsumi et al ("Utsumi"). As discussed above, amended independent claims 1 and 17 are patentably distinguishable over Giri, Naya, and Tanaka and, as such, claim 5 depending from amended independent claim 1 and claim 21 depending from amended independent claim 17 are, *a fortiori*, also patentably distinguishable over Giri, Tanya, and Tanaka, for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The Examiner has further rejected claims 16 and 32 under 35 USC §103(a) as being unpatentable over Giri in view of Naya and Tanaka, and further in view of U.S. patent number 5,886,589 to Jean-Marc Mourant. As discussed above, amended independent claims 1 and 17 are patentably distinguishable over Giri, Naya, and Tanaka and, as such, claim 16 depending from amended independent claim 1 and claim 32 depending from amended independent claim 17 are, *a fortiori*, also patentably distinguishable over Giri, Tanya, and Tanaka, for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1 and 17 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-5, 7-21, and 23-32 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-5, 7-21, and 23-32 pending in the present application is respectfully requested.

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Respectfully Submitted,
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